[0020] In some example embodiments, a center line of the signal metal patterns and a center line of the dummy metal pattern may coincide with each other along the straight line.

[0021] In some example embodiments, the metal wiring may include a plurality of signal metal patterns being parallel to each other, the signal metal patterns including the signal metal pattern, the dummy metal pattern may be parallel to the signal metal patterns and is between the signal metal patterns, and a distance between the dummy metal pattern and one of the signal metal patterns is substantially same as a distance between the dummy metal pattern and another of the signal metal patterns.

[0022] In some example embodiments, the signal metal patterns may have different widths, and the dummy metal pattern may have a width substantially same as the shortest width among the widths of the signal metal patterns.

[0023] In some example embodiments, the metal wiring may include a plurality of dummy metal patterns arranged between the signal metal patterns, the dummy metal patterns may include the dummy metal pattern, and a distance between the dummy metal patterns may be substantially same as the distance between the dummy metal pattern and the signal metal pattern.

[0024] According to an example embodiment, a metal wiring of a semiconductor device includes at least one signal metal pattern in a peripheral region of a semiconductor substrate, the at least one signal metal pattern electrically connected to a circuit of the semiconductor substrate, and at least one dummy metal pattern in the peripheral region and filling regions unoccupied by the at least one signal metal pattern, the at least one dummy metal pattern electrically insulated from the circuit of the semiconductor substrate, the at least one dummy metal pattern having a width substantially same as a width of the at least one signal metal pattern, a distance between neighboring two from among the at least one dummy metal pattern and the at least one signal metal pattern being substantially same as a distance between cell metal patterns in a cell region.

[0025] In some example embodiments, the at least one signal metal pattern may be parallel to the at least one dummy metal pattern.

[0026] In some example embodiments, the at least one signal metal pattern may include a first signal metal pattern, and a second signal metal pattern and the at least one dummy metal pattern may be between the first and second signal metal patterns such that center lines of the first and second metal lines and a center line of the at least one dummy metal pattern form a straight line.

[0027] In some example embodiments, a first distance between the first signal metal pattern and the at least one dummy metal pattern may be substantially same as a second distance between the second signal metal pattern and the at least one dummy metal pattern.

[0028] In some example embodiments, the at least one signal metal pattern may include a plurality of signal metal patterns having different widths, and the at least one dummy metal pattern may have a width substantially same as a shortest width from among the signal metal patterns.

[0029] According to an example embodiment, the second mask pattern for forming the dummy metal pattern in the peripheral region of the semiconductor substrate may be arranged between the first mask patterns for forming the signal metal pattern in the peripheral region of the semiconductor substrate. The width of the second mask pattern may be substantially the same as the width of the first mask pattern. Thus, the metal wiring in the peripheral region formed using the mask may have a minute and uniform pitch corresponding to a pitch of the metal wiring in the cell region. As a result, the metal wiring in the peripheral region using the mask and an off-axis illumination may have a designed shape and size so that a short between the metal wirings and/or a cut of the metal wiring in the peripheral region may be inhibited or prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGS. **1** to **15** represent non-limiting, example embodiments as described herein.

[0031] FIG. **1** is a plan view illustrating a mask in accordance with an example embodiment;

[0032] FIG. **2** is an enlarged plan view of a portion "II" in FIG. **1**;

[0033] FIG. **3** is an enlarged plan view of a portion "III" in FIG. **1**;

[0034] FIG. **4** is an enlarged plan view of a portion "IV" in FIG. **1**,

[0035] FIG. **5** is an enlarged plan view of a portion "V" in FIG. **1**;

[0036] FIG. **6** is an enlarged plan view of a portion "VI" in FIG. **1**;

[0037] FIGS. **7** to **9** are cross-sectional views illustrating a method of forming a metal wiring of a semiconductor device using the mask in FIG. **1**, according to an example embodiment;

[0038] FIG. **10** is a plan view illustrating a metal wiring of the semiconductor device using the mask in FIG. **1**;

[0039] FIG. **11** is an enlarged plan view of a portion "XI" in FIG. **10**;

[0040] FIG. **12** is an enlarged plan view of a portion "XII" in FIG. **10**;

[0041] FIG. **13** is an enlarged plan view of a portion "XIII" in FIG. **10**;

[0042] FIG. **14** is an enlarged plan view of a portion "XIV" in FIG. **10**; and

[0043] FIG. **15** is an enlarged plan view of a portion "XV" in FIG. **10**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0044] Various example embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some example embodiments are shown. The present inventive concepts may, however, be embodied in many different forms and should not be construed as limited to the example embodiments set forth herein. Rather, these example embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present inventive concepts to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity.

[0045] It will be understood that when an element or layer is referred to as being "on," "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is